

**PATENT APPLICATION****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re application of

Docket No: 002187 USA/C03/PDC/WF/OR  
(CA1120)

David ALUMOT, et al.

**RECEIVED  
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Appln. No.: 09/765,995

Group Art Unit: 2623

SEP 22 2004

Confirmation No.: 1810

Examiner: Mehrdad Dastourj

Filed: January 19, 2001

For: **OPTICAL INSPECTION APPARATUS FOR SUBSTRATE DEFECT DETECTION****APPEAL BRIEF UNDER 37 C.F.R. § 41.37****MAIL STOP APPEAL BRIEF - PATENTS**Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellants within a four (4) month period from the May 24, 2004, filing date of the Notice of Appeal, extended by concurrent filing of a petition for two-month extension of time and payment of fee, submit the following:

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**I. REAL PARTY IN INTEREST**

The real party in interest here is the owner of the application, Applied Materials, Inc.

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**II. RELATED APPEALS AND INTERFERENCES**

To the best of their knowledge, Appellants are not aware of any other appeals or interferences involving the present application.

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**III. STATUS OF CLAIMS**

Claims 96-105 are all the claims pending in the application. All claims are rejected. All claims are appealed.

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**IV. STATUS OF AMENDMENTS**

The claims have not been amended pursuant to final rejection.

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**V. SUMMARY OF THE CLAIMED SUBJECT MATTER**

The present invention provides an apparatus for inspecting patterned semiconductor wafers at high speed and with a relatively low false alarm rate.

The inspection is made in two phases. As shown in Fig. 1, in the first phase, the complete surface of a wafer W is inspected at a relatively high speed and with a relatively low spatial resolution. A plurality of light collectors 4 collect the light scattered from the wafer W and to transmit the scattered light to a plurality of detectors 5. A phase I image processor 7 processes the outputs of the detectors 5 and produces information indicating suspected locations on the wafer having a high probability of a defect.

As shown in Fig. 12, the phase I image processor includes an input from each of the eight sensors 46a - 46g and 46r to their respective preprocessors 6a - 6g and 6r. The sensors convert the light signals to analog electrical signals, and the preprocessors sample the latter signals at pixel intervals and convert them to digital data.

In Fig. 14, a threshold processor 70 receives the pixel stream from the scanned object via its preprocessor, e.g., 6a, and outputs its threshold levels to a pixel characterizer 72 for registration and to a pixel characterizer 74 for comparison.

A comparator 77 has four inputs: reference pixels input (a) corresponding to the intensity of the pixels in the reference image; reference type input (b) corresponding to the type of pixel in the reference image; inspected type input (c) corresponding to the type of the pixels in the

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inspected image; and inspected pixels input (d) corresponding to the intensity of pixels in the inspected image. Detection of defects is based on the comparison of each pixel in the inspected stream with the corresponding pixel in the corresponding reference stream. Pixels are compared relative to an adaptive threshold determining detection sensitivity according to pixel type.

Two flows of eight streams of data are generated: one flow represents the pixels of eight different images of the reference pattern; and the other flow represents the pixels of different images of the inspected pattern to be compared with those of the reference pattern in order to provide an indication of the presence of a defect in the inspected pattern.

Only the suspected locations having a high probability of a defect are examined by the Phase II examining system. The Phase II examining system includes an optic system for imaging the suspected location on an opto-electric converter, e.g., a CCD matrix 9, which converts the images to electric signals. The signals are fed via a phase II preprocessor 10 to a phase II image processor 11, which, under the control of the main controller 8, outputs information indicating the presence or absence of a defect in each suspected location examined in Phase II.

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**VI.  GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

1. Claims 96, 97, 100, 101, 104, and 105 stand rejected under 35 U.S.C. §103(a) as being unpatentable over USP 4,764,969 to Ohtombe et al. in view of USP 5,185,812 to Yamashita et al.
2. Claim 98 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Ohtombe and Yamashita, further in view of USP 4,791,586 to Maeda et al.
3. Claims 99 and 102 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ohtombe, Yamashita, and Maeda, further in view of USP 4,618,938 to Sandland et al.
4. Claim 103 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Ohtombe and Yamashita, further in view of Sandland.

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**VII. ARGUMENTS**

**The Prior Art**

**Ohtombe**

Ohtombe provides an apparatus capable of automatically performing both macroscopic whole inspection and microscopic point inspection without the need for human visual inspection. Ohtombe locates defect positions on a wafer surface by comparing brightness differences between reflections from unusual and normal portions on the surface.

As shown in Ohtombe Fig. 1, the Ohtombe apparatus comprises a macroscopic inspecting section A for inspecting a whole wafer surface, and a microscopic inspecting section B for inspecting particular points of the wafer surface. In the macroscopic inspecting section A, a wafer 1 is irradiated almost horizontally by light from a light source 3. Images of the wafer surface by reflection are fed from an industrial TV camera 4 to an image processing section 5.

The image processing section 5 processes and analyses images entered from the industrial TV camera 4 using a preset procedure with a difference of diffuse reflection and Miller surface reflection, thus detecting unusual positions on the wafer surface (Ohtombe, col. 2, lines 44-66). If there is a scratch or a defect on the surface of the wafer 1, the scratch or the defect causes diffuse reflection. On the other hand, the remaining portions of the surface cause Miller reflection. The images of unusual positions appear brighter than those of the normal surface (Ohtombe, col. 4, lines 39-45).

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As shown in Fig. 3, referred to by the Examiner, the image processing section 5 comprises an A/D conversion section 41, a memory section 43 and a comparison section 45. The A/D conversion section 41 converts analog image data from the ITV camera 4 to digital image data, and sections the digital image data like a mesh to fit masked pattern shown in Fig. 2. The memory section 43 has information of threshold values in accordance with sectioned portions shown in Fig. 2. The comparison section 45 compares the digital value generated by A/D conversion section 41 with the threshold value of the memory section 43.

**Yamashita**

Yamashita provides an apparatus to avoid detecting dimensional errors due to rounded corners of a circuit pattern and thinning or fattening of line widths and a positioning error of an examination table as defects (Yamashita, col. 1, lines 52-55). Yamashita solves the false defect detection problem by equipping a pattern inspection apparatus with a pattern feature extracting function which permits extraction of features of a circuit pattern including edges and corners (Yamashita, col. 2, lines 12-22).

In Fig. 1B of Yamashita, an image data sensor 13 obtains images data of the inspected pattern. The image data is converted to a multivalued digital signal by an A/D converter 14. An arithmetic unit 17 subtracts reference pattern data from a data converter 16 from the multivalued digital signal from the A/D converter 14, and the resultant difference is applied to a comparator 18. The comparator 18 is provided with a spatial differentiation filter to obtain the minimum and maximum of the difference between the inspected pattern from the A/D converter 14 and the

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design pattern from the data converter 16. The output of the comparator 18 is applied to a defect determining circuit 19 which, when at least one of the absolute value of the density difference, the minimum and the maximum exceeds its corresponding threshold, is adapted to determine a defect.

**Prosecution history**

The present application is a continuation application of U.S. patent application No. 09/298,501, which has matured into USP 6,178,257 (the '257 patent).

In an Office Action dated August 27, 2002, the previous Examiner rejected claims 96, 100, 101, and 104 as being anticipated by Ohtombe. That Examiner asserted that the comparison section 45 of Ohtombe teaches the recited comparator, referring to Fig. 2, and col. 3, lines 48-55 of Ohtombe.

During a telephone interview with the previous Examiner on October 28, 2002, Appellants brought the following to his attention:

- 1) Both independent claim 96 of the present application and claim 6 (application claim 128) of the '257 patent, parent of the present application, contain similar limitations as to the comparator.
- 2) The Examiner of the '257 patent had rejected application claim 128 based on the Ohtombe reference on which the previous Examiner relied here.

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3) Appellants traversed that prior art rejection in the '257 patent successfully, arguing that Ohtombe fails to teach or suggest obtaining a different between the inspection data and reference data.

As a result of the interview, the previous Examiner of the present application agreed that amendments to dependent claim 104 in response to a 35 U.S.C. §112, second paragraph rejection and a Terminal Disclaimer would put the present application in an allowable condition.

Appellants filed a Terminal Disclaimer and an Amendment on December 11, 2002.

In an Office Action dated May 28, 2003, the previous Examiner withdrew the 35 U.S.C. §102(b) rejection as to claim 96, but rejected claim 96 under 35 U.S.C. §103(a) as being unpatentable over Ohtombe and Yamashita, asserting that Ohtombe discloses every limitation of claim 96, except for the comparator calculating the difference between the inspection signals and a reference signal, but Yamashita supplies the deficiencies. The previous Examiner referred to Fig. 1B of Yamashita, asserting that the data comparator 18 teaches the recited comparator, the A/D converter 14 provides inspected signals, and the reference data converter 16 provides the reference signal.

Appellants argued that it is improper to combine Ohtombe and Yamashita, because given the completely different solutions used by the two references, and the lack of any need for a reference signal or a comparator calculating a difference between inspection signals and a reference signal in Ohtombe, there would be no reason to combine these two references.

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Appellants also argued that both Ohtombe and Yamashita were in front of the Examiner of the '257 patent, who applied the Ohtombe reference and Yamashita reference separately against different claims, apparently recognizing the non-combinability of Ohtombe and Yamashita.

Appellants further argued that a skilled artisan would not be able to incorporate the Yamashita comparator into the Ohtombe apparatus without substantially changing the principle of operation of the references and substantially redesigning the construction of the references, because Ohtombe detects defects by a difference in brightness between diffuse reflection caused by unusual portions and Miller surface reflection caused by normal portion, while Yamashita avoids false defect detection by comparing image data representing the distribution of density of a two-dimensional inspected pattern and a pre-stored reference pattern data representing a typical pattern of a circuit pattern.

In an Office Action dated December 22, 2003, the previous Examiner maintained the claim rejections.

In a Response dated March 22, 2004, Appellants further explained why it is improper to combine Ohtombe and Yamashita.

In the Advisory Action, the current Examiner stated that Yamashita was merely cited to further identify the abstract concept corresponding to the details of calculating a difference between an inspection signal and a reference signal.

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**Arguments for Patentability**

The current Examiner has agreed that Ohtombe fails to teach or suggest calculating a difference between inspection signals (output of the A/D converter 41), and reference signals (threshold values stored in memory 43), but asserts that Yamashita provides an abstract concept corresponding to the details of calculating a difference between an inspection signal and a reference signal. Appellants respectfully disagree.

As Appellants argued during prosecution of the '257 patent, the comparator in claim 96 calculates a difference between inspection signals and a reference signal to identify locations on substrate suspected of having defects thereupon based on a threshold. The reference signal and the threshold are two different limitations. As shown in Fig. 14 of the present application, threshold signals are from the threshold processor 70, while reference signals are from reference die memory 75.

In the Office Action dated December 22, 2003, page 4, the first paragraph, the previous Examiner asserted that the values held in the memory 43 in Fig. 3 of Ohtombe teach the recited threshold. However, in the Advisory Action, page 2, the third paragraph, the current Examiner has asserted that the threshold values stored in the memory 43 in Fig. 3 of Ohtombe correspond to the recited reference signals. Appellants submit that it is improper for the Examiners to read the threshold values stored in the memory 43 of Ohtombe on both the recited reference signal and the recited threshold.

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The current Examiner reads values stored in the memory 43 of Ohtombe on the recited reference signals, but has not pointed out which part in Ohtombe teaches the recited threshold.

Appellants have difficulty understanding the current Examiner's position regarding the alleged teaching of the prior art. On one hand, the current Examiner asserts that the threshold values stored in memory 43 of Ohtombe correspond to the recited reference signals, the comparison section 45 of Ohtombe corresponds to the recited comparator, and the signals from the A/D conversion section 41 corresponds to the recited inspection signals. On the other hand, the current Examiner has asserted that Ohtombe does not teach calculating a difference between inspection signal (A/D converter 41 output signal) and reference signals (threshold values stored in memory 43), although Ohtombe explicitly teaches that the comparison section 45 compares the threshold values stored in memory 43 and the signals from the A/D conversion section 41.

In the Advisory Action, page 2, the third paragraph, the current Examiner agreed that Ohtombe does not disclose calculating a difference between inspection signals and reference signals, but at the same time asserted that Ohtombe teaches the recited comparator. Appellants disagree. In claim 96, the comparator is used to calculate a difference between inspection signals and a reference signal. It is impossible for Ohtombe to teach the recited comparator without teaching its function.

Further, the current Examiner has asserted that incorporation of the Yamashita comparator into the Ohtombe apparatus would not substantially change the principle of operation

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of the references and would not substantially redesign the construction of the references.

Appellants respectfully disagree.

As discussed above, the comparison section 45 in Fig. 3 of Ohtombe compares the digital values generated by the A/D conversion section 41 with the threshold value of memory section 43, and sends the output to a CPU 49. Both Examiners who have handled the present application have asserted that the comparison section 45 corresponds to the recited comparator, signals from the A/D converter 41 correspond to the recited inspection signals, and threshold stored in the memory 43 correspond to the recited threshold and the recited reference signals. In Appellants' view, neither path that the Examiners have taken to read the claims of the present application on the prior art is properly discernible, for the following reasons:

- 1) If the threshold stored in the memory 43 corresponds to the recited threshold, as the previous Examiner suggested, there is no reason for a skilled artisan to modify Ohtombe to further calculate a difference between the signals from the A/D converter 41 and a reference signal, because comparison of the threshold stored in the memory 43 and signals from the A/D converter 41 is enough to locate the defect.
- 2) If the threshold stored in the memory 43 corresponds to the recited reference, as the current Examiner has asserted, then there is no part of Ohtombe which teaches the threshold, or how or why the ordinarily skilled artisan would even find it

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necessary to pick a threshold from another reference to add to Ohtombe, much less how to make that modification.

Even if a skilled artisan were to incorporate the Yamashita comparator into the Ohtombe apparatus, as the Examiners suggested, Appellants can not see how he/she could modify Ohtombe to obtain the invention of claim 96. For example, if the threshold values stored in the memory 43 of Ohtombe correspond to the recited threshold, as the previous Examiner suggested, then there is no teaching or suggestion of where to get the reference signal, what will the reference signal stand for, how to use the difference to improve the performance of the Ohtombe apparatus. If the threshold values stored in the memory 43 of Ohtombe correspond to the recited reference signal, as the current Examiner has suggested, then there is no teaching or suggestion of where to get the threshold, what will the threshold stand for, how to use the difference to improve the performance of the Ohtombe apparatus/

As Appellants argued previously, Ohtombe analyses brightness differences between reflections from unusual and normal portions on the surface of a substrate to locate defects, while Yamashita compares density differences of signals to detect defects. The necessary modifications to Ohtombe are not suggested by Yamashita, and vice versa. Thus, Appellants resubmit that there is no suggestion or motivation for a skilled artisan to combine these two references, and there is not reasonable expectation of success either. Accordingly, Appellants submit that claim 96 and its dependent claims 97-105 are patentable.

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**Conclusion**

Pursuant to the foregoing arguments, Appellants submit that claims 96-105 are patentable. Accordingly, Appellants respectfully request that the Examiner's rejection be reversed, and the present application allowed at the earliest possible opportunity.

Unless a check is submitted herewith for the required fee, please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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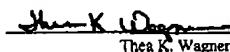
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Date: September 22, 2004

**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that this APPEAL BRIEF UNDER 37 C.F.R. § 41.37  
is being facsimile transmitted to the U.S. Patent and Trademark Office  
this 22<sup>nd</sup> day of September, 2004.



Thea K. Wagner

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**CLAIMS APPENDIX**

**CLAIMS 96-105 ON APPEAL:**

96. An apparatus for inspection of a substrate, said apparatus comprising:
  - an illumination source illuminating said substrate;
  - first collection optics receiving light and outputting inspection signals;
  - a comparator calculating a difference between said inspection signals and a reference signal to identify locations on said substrate suspected of having defects thereupon based on a threshold, and outputting suspect location data;
  - second collection optics receiving light and outputting images according to said suspect location data; and
  - a defect classifier receiving and classifying said images.
97. The apparatus of claim 96, wherein said illumination source is a laser.
98. The apparatus of claim 96, wherein said first collection optics comprises a plurality of sensors.
99. The apparatus of claim 98, wherein said first collection optics further comprises dark field collection optics.
100. The apparatus of claim 96, wherein said second collection optics comprises an imaging sensor.

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101. The apparatus of claim 100, wherein said second collection optics further comprises bright field collection optics.

102. The apparatus of claim 99, wherein said dark field collection optics includes a turret carrying a plurality of objectives thereupon.

103. The apparatus of claim 101, wherein said bright field collection optics includes a turret carrying a plurality of objectives thereupon.

104. The apparatus of claim 96, further comprising an image processor receiving an output of said second collection optics and outputting said images.

105. The apparatus of claim 96, wherein said threshold is an adaptive threshold.

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**EVIDENCE APPENDIX**

None.

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***RELATED PROCEEDINGS APPENDIX***

None